Low Temperature Transport of C_{60} thin film FET

Kazunaga Horiuchi [a,b], Shin Uchino [a], Kenji Nakada [a], Nobuyuki Aoki [a], Masaaki Shimizu [b], Yuichi Ochiai [a,1]

[a] *Department of Materials Technology, Chiba University, 1-33 Yayoi, Inage, Chiba 263-8522, Japan*
[b] *Corporate Research Center, Fuji-Xerox Co. Ltd., 430 Sakai, Nakai, Ashigarakami-gun, Kanagawa 259-0157, Japan*

Abstract

Electrical conduction properties of C_{60} thin-film field-effect transistor (FET) grown at room temperature was investigated with various gate voltages. The conduction property was explained by thermal activation, which was strongly dependent on the gate voltages in a high temperature regime above 260K. Caluculated activation energies decreased as the gate voltage increased and saturated below 0.4 eV at high gate voltages.

Key words: C_{60}; thin-film; Field-effect Transistor; Thermal Activation

1. Introduction

It is well known that C_{60} thin-film behaves as a n-type semiconductor and shows relatively high mobility in comparison with other organic materials. In a recent field-effect transistor (FET), the gate voltage can introduce an electric field to the C_{60} thin-film and modulate the conduction characteristics by more than 10^4 orders of conduction magnitude. Especially the conduction mobility shows as high as 0.1 cm^2/Vs. In recent reports [1–6] for oligothiophenes, pentacene and polythienylene vinylene, those conduction mobilities of organic FETs show clear dependences on the gate voltage, which indicate that the not only the charge density but also the transport mechanism might be affected by electric fields. Several models have been proposed to explain the gate dependence; localized polaron-like state [1], variable range hopping for exponentially distributed traps [2], extended state conduction with multiple trapping and release [3–5], energy barriers at grain boundary [4,5] or charge concentration effect at a semiconductor-insulator interface [4–6].

In this research we measured transport characteristics as a function of temperature with various gate voltages. A poly-crystalline C_{60} thin-film FET was intensionally used to investigate the gate dependence mainly affected by grain boundaries.

2. Sample and experiment

C_{60} Thin-film was evaporated in a high vacuum with a pre-purified C_{60} source by liquid-chromatography to separate residual constituents. Heavily doped p-type silicon wafer was used for a substrate in order to act as a back gate electrode with topping of an insulating layer of thermally grown silicon dioxide about 500 nm. The substrate's temperature was kept around room temperature to obtain a poly-crystalline phase for C_{60} FET. Channel electrodes of Au/Ti were patterned on the substrate in sizes of 85 mm (width) and 40 mm (gap). Before conduction measurements, the sample was annealed in a high vacuum chamber at 400K to exculude adsorbed oxygen for more than 10 hours. The chamber was equipped with current-probe manipulators and liquid-He cooling cryostat, which enables successive conduction measurements after the sample annealing. The sample was stabilized for 30 min at each

[1] Corresponding author. E-mail: ochiai@xtal.tf.chiba-u.ac.jp

temperature to avoid current fluctuation by a heat flow.

3. Results and discussion

Arrhenius plots of electrical conductions of C_{60} thin-film FET are shown in Fig.1 as a function of 1000/T with various gate voltages . For each gate voltage the conduction decreases as the temperature is lowered. There is no saturation region at low temperature as reported in Ref [3,5], in which saturation behavior was attributed to a band-like conduction. The conduction behavior in Fig.1 can be classified into 3 regimes; high temperature (HT) regime above 260 K, intermediate temperature (MT) regime from 260 to 200 K and low temperature (LT) regime below 200 K. The conduction seems to depend strongly on the gate voltage for HT regime. The transport in MT regime is complicated because of an influence by a phase transition around 256K that is typical property for C_{60} materials to change the structure from face centered cubic to simple cubic.

In both HT and LT regimes, a thermal activation model has been applied for the conduction behaviors so as to fit a straight line as shown in Fig.1. Activation energies estimated for each regime are plotted as a function of gate voltages in Fig.2. The activation energies become saturate for both regimes at high gate voltages. A strong dependence on gate voltages is clearly seen for HT regime and the value varies in a wide range from 0.3 eV to 1.4 eV. On the other hand, a weak dependence is seen for LT regime. It may come from the phase transition through MT regime, but it is not so clear because of a lack of data for low gate voltages in LT regime.

The strong gate dependence at the HT regime seems difficult to explain with a half value of measured optical band gap of 2.3 eV [7] or carrier trapping sites in the band gap. Therefore, we should assume an energy barrier at grain boundary in order to suppress the electron transport. However, another possibility can not be denied for a certain energy barrier due to a contact resistance at the interface region around electrode. If we introduce the energy barrier, we must consider both for intergrain transport via the grain boundary and intragrain transport inside the grain. For our future problems, we must clarify the gate voltage dependences further more clearly on the transport for the inside of the grain using a single-crystalline sample.

4. Summary

Electrical conduction properties of C_{60} thin-film FET has been investigated with various gate voltages.

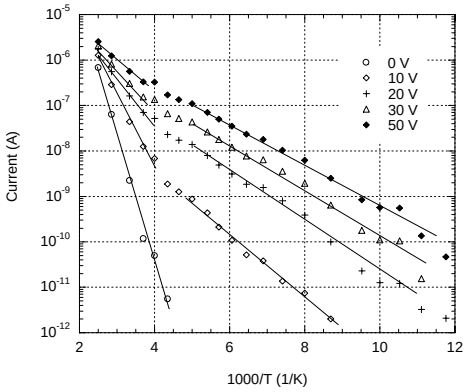

Fig. 1. Arrhenius plots of electric conductions of C_{60} thin-film FET as a function of 1000/T are shown with various gate voltages. Straight lines are added to indicate thermal activation conductions.

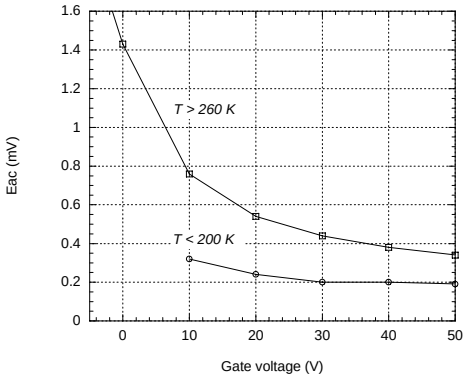

Fig. 2. Activation energies derived from straight lines shown in Fig 1. are plotted for different temperature regimes.

Conductance decreases as the temperature is lowered for all temperature range. A strong dependence on the gate voltage has been observed for the conduction in HT regime, which is probably attributed to an energy barrier at grain boundary.

References

[1] A. Brown, C. Jarrett, D. de Leeuw, M. Matters, Synth. Met. **88** (1997) 37.

[2] M. Vissenberg, M. Matters, Phys. Rev. B**57** (1998) 12964.

[3] G. Horowitz, R. Hajalaoui, R. Bourguiga, M. Hajalaoui, Synth. Met. **101** (1999) 401.

[4] G. Holowitz, R. Hajalaoui, D. Fichou, A. Kassmi, J. Appl. Phys. **85** (1999) 3202.

[5] G. Horowitz, M. Hajalaoui, R. Hajalaoui, J. Appl. Phys. **87** (2000) 4456.

[6] J. Schön, B. Batlogg, J. Appl. Phys. **89** (2001) 336.

[7] R. Lof, M. Veenendaal, B. Koopmans, H. Jonkman, G. Sawatzky Phys. Rev. Lett. **68** (1992) 3924.