Effects of local gates on the electrical transport of single-walled carbon nanotubes

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Abstract

We have studied the effect of local gates on the electrical transport properties of single-walled carbon nanotubes. The local gate have been incorporated into individual single-walled carbon nanotube by depositing Al top gate in between Au/Ti electrodes. Noticeable increase of resistance was observed after the deposition of the Al top gates, implying that the Al top gate acted as a barrier for electrical conduction.

Key words: Carbon nanotube, single-electron tunneling, field effect transistor

1. Introduction

A variety of carbon nanotube-based electronic devices, such as field effect transistor (FET) [1,2] and single-electron transistor (SET) [3–5], have been realized and investigated. Single-electron tunneling effect was initially observed in an individual metallic single-walled carbon nanotube (SWNT) device with high-resistance contacts [3]. The quantum dot was considered to be formed in the segment of the SWNT in between the two electrodes. Later, another methods to define quantum dot in a SWNT were proposed and realized [6–8]. One of the key issues in this field is to find more controllable and reliable method to define quantum dot for SET and local gate for FET. In this paper, we present a method to incorporate local gates to individual SWNTs. We have adopted the dual-gate structure consisting of two line-shaped Al top gates and a back gate. The top gates induce local deformations acting as conduction barriers and multi quantum dots are formed underneath the Al top gate.

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2. Results

The SWNTs used in this study were synthesized by the chemical vapor deposition method. Atomic force microscope study revealed that the diameter of SWNT was about 2 nm. The SWNTs were ultrasonically dispersed and spin coated on the degenerately doped Si substrate with a 100 nm-thick thermally grown SiO_2 layer. The Au/Ti (50/20 nm) electrodes were made by using electron beam lithography and lift-off technique and a rapid thermal annealing was performed at 800°C for 30 s in vacuum to form good contacts between SWNT and the metal electrodes. The room temperature resistance of the sample were several tens of kΩ. Electrical transport measurement was performed before depositing Al top gate. Then the sample was taken out of the cryostat, and Al top gates were incorporated between Au/Ti electrodes, as shown schematically in the inset of Fig. 1. The width and the thickness of Al gates were about 200 nm and 100 nm, respectively, and the spacing between two Al gates about 200 nm. There was no leakage current between Al and Au/Ti electrodes up to 5 V.

Figure 1 shows the current-voltage($I - V$) curves measured at 4.2 K before (dotted line) and after (solid line) the deposition of the Al top gates. In both cases energy gap was observed, suggesting semiconducting behavior of the SWNT. The resistance increased more than 10 times after the Al deposition and weak step-like structures were manifested in the $I-V$ characteristics. The Al top gate was expected to induce local deformation acting as a barrier for electron conduction, which explains the increase of resistance after the deposition of the Al top gates.

The dash line in Fig. 1 is the $I-V$ curve with the application of 1 V commonly to the two Al top gates. The current decreased with the application of positive bias voltage to the top gates, indicating a $p-$type semiconducting behavior of the SWNT. This is also confirmed by the back-gate modulations shown in the inset of Fig. 2. We have compared in Fig. 2 the gate modulations with the back gate (inset) and the Al top gate (main panel). The rate of current decrease was far greater for Al top gate than the back gate. This is an expected result because the Al top gate contacts directly on the SWNT while the back gate is separated with the SWNT by 100 nm-thick SiO_2 layer.

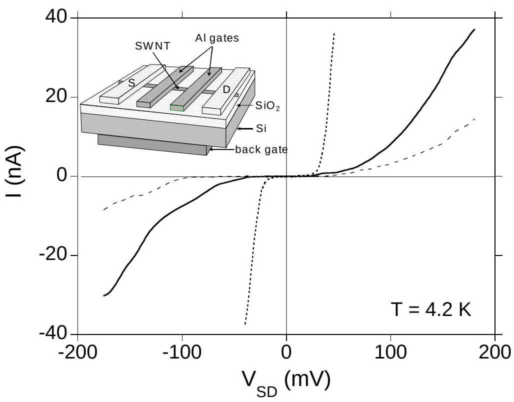

Fig. 1. The $I-V$ characteristics before (dotted line) and after (solid line) the deposition of Al top gate. The dash line is the $I-V$ characteristics after the deposition of Al top gate with the application of the top-gate voltage of 1 V. Inset shows the schematics of the device.

Fig. 2 shows the top-gate modulations at 4.2 K with the source-drain voltages from 20 mV to 80 mV in step of 20 mV. Complete current suppression was observed for top-gate voltage (V_{TG}) greater than 0.5 V. In addition to such $p-$type field effect, also observed was nearly periodic oscillation of source-drain current with varying the top-gate voltage. Such current oscillation, a typical behavior of single-electron transistor, strongly suggests possible formation of quantum dot in the SWNT. Note that the back-gate modulation shown in the inset of Fig. 2 exhibits no current oscillation. These experimental observations suggests that in addition to the local deformation induced by deposited Al, application of bias voltage is essential for the formation of quantum dot in the SWNT.

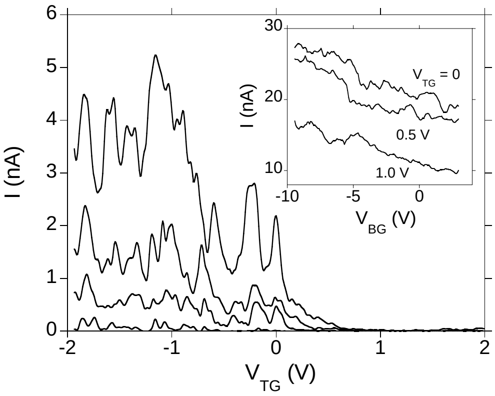

Fig. 2. The top-gate modulations at 4.2 K with the source-drain voltages from 20 mV to 80 mV in step of 20 mV. Inset shows the back-gate modulations with varying top-gate voltages.

3. Summary

In sum, we have fabricated a SWNT-based electronic device with two line-shaped Al top gates in between source and drain electrodes. It has been shown that the Al top gate can be used as a local gate for FET and SET.

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