Experimentally realizable scalable quantum computing using superconducting qubits

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Abstract

We propose an experimental method to implement scalable quantum computing (QC) in which any two charge qubits can be effectively coupled by an experimentally accessible inductance. We formulate an efficient and realizable QC scheme that requires only one (instead of two or more) two-bit operation to implement conditional logic gates.

Key words: quantum computing; superconducting Josephson charge qubits

1. Introduction

Josephson-junction circuits have received much attention because they may be used in quantum computing (QC) [1]. Based on the charge and phase degrees of freedom in the Josephson-junction devices, charge [2,3] and phase qubits [4,5] have been developed. Also, a new type of solid-state qubit is realized in a current-biased Josephson junction [6]. Recent experiments [2,5–7] has shown that the Josephson qubits are very promising in manufacturing quantum information processors.

Here we present an experimental method to implement QC using Josephson charge qubits. A common inductance is used to directly couple the charge qubits involved, in contrast with the scheme in [3] where oscillating modes in LC circuits are employed to generate interbit coupling. Our QC architecture is scalable in the sense that any two charge qubits (not necessarily neighbors) can be effectively coupled by an experimentally accessible inductance. More importantly, we formulate an *efficient* QC scheme that requires only one two-bit operation to implement conditional logic gates.

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2. Quantum-computer structure

The proposed quantum computer consists of N Cooper-pair boxes coupled by a common superconducting inductance L (see Fig. 1). For the kth Cooper-pair box, a superconducting island with excess charge $Q_k = 2en_k$ is weakly coupled by two symmetric dc SQUIDs and biased by an applied voltage V_{Xk} through a gate capacitance C_k. The two symmetric dc SQUIDs are assumed to be identical and all Josephson junctions in them have Josephson coupling energy E^0_{Jk} and capacitance C_{Jk}. The magnetic fluxes through the two SQUID loops of the kth Cooper-pair box are designed to have the same values Φ_{Xk} but opposite directions, so that this pair of fluxes cancel each other in any loop enclosing them. The coupling of selected Cooper-pair boxes by the common superconducting inductance L can be implemented by switching on the SQUIDs connected to the chosen Cooper-pair boxes.

For any given Cooper-pair box, say i, when $\Phi_{Xk} = \frac{1}{2}\Phi_0$ and $V_{Xk} = (2n_k + 1)e/C_k$ for all boxes except $k = i$, the inductance L only connects the ith Cooper-pair box to form a superconducting loop. In the spin-$\frac{1}{2}$ representation with charge states $|\uparrow\rangle_i \equiv |n_i\rangle$ and $|\downarrow\rangle_i \equiv |n_i + 1\rangle$, the reduced Hamiltonian

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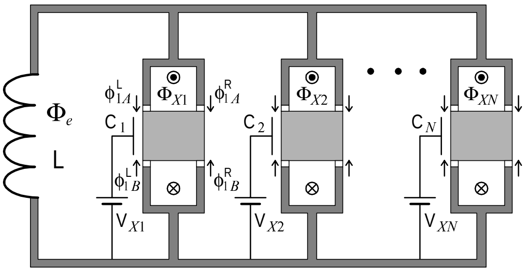

Fig. 1. Schematic diagram of the proposed scalable quantum computer. Each Cooper-pair box is operated in the charging regime with E_{ck} much larger E^0_{Jk}, $k = 1, 2, \ldots, N$. Also, $k_B T \ll E_{ck} < \Delta$ (the superconducting gap).

of the system is $H_1 = \varepsilon_i(V_{Xi})\,\sigma_z^{(i)} - \overline{E}_{Ji}\,\sigma_x^{(i)}$, where $\varepsilon_i(V_{Xi}) = \frac{1}{2}E_{ci}[C_i V_{Xi}/e - (2n_i + 1)]$, with $E_{ci} = 2e^2/(C_i + 4C_{Ji})$. The intrabit coupling $\overline{E}_{Ji}$ is given by $\overline{E}_{Ji} = E_{Ji}(\Phi_{Xi})\cos(\pi\Phi_e/\Phi_0)\xi$, where $E_{Ji}(\Phi_{Xi}) = 2E^0_{Ji}\cos(\pi\Phi_{Xi}/\Phi_0)$, and $\Phi_0 = h/2e$. Here, ξ is a power series with expansion parameter $\eta_i = \pi L I_{ci}/\Phi_0$, where $I_{ci} = -\pi E_{Ji}(\Phi_{Xi})/\Phi_0$. Retained up to second-order terms, $\xi = 1 - \frac{1}{2}\eta_i^2\sin^2(\pi\Phi_e/\Phi_0)$. This two-level system is somewhat similar to the charge-flux qubit [7] because it involves both the charge states and the flux in the loop.

To couple *any* two Cooper-pair boxes, say i and j, we choose $\Phi_{Xk} = \frac{1}{2}\Phi_0$ and $V_{Xk} = (2n_k + 1)e/C_k$ for all boxes except $k = i$ and j. The inductance L is shared by the Cooper-pair boxes i and j to form superconducting loops, and the reduced Hamiltonian of the system is $H_2 = \sum_{k=i,j}[\varepsilon_k(V_{Xk})\,\sigma_z^{(k)} - \overline{E}_{Jk}\,\sigma_x^{(k)}] - \chi_{ij}\,\sigma_x^{(i)}\sigma_x^{(j)}$. Up to second-order terms, the intrabit coupling is $\overline{E}_{Ji} = E_{Ji}(\Phi_{Xi})\cos(\pi\Phi_e/\Phi_0)\xi$, with $\xi = 1 - \frac{1}{2}(\eta_i^2 + 3\eta_j^2)\sin^2(\pi\Phi_e/\Phi_0)$, and the interbit coupling is $\chi_{ij} = L I_{ci} I_{cj}\sin^2(\pi\Phi_e/\Phi_0)$. Here we assume that the inductance of the qubit circuits is much smaller than L. When the two qubits are far apart, the inductance of the wires connecting them might not be neglected. However, the reduced two-bit Hamiltonian is still given by H_2, but with $\overline{E}_{Jk}$ and χ_{ij} slightly modified.

3. Universal set of quantum logic gates

A quantum system evolves according to $U(t) = \exp(-iHt/\hbar)$. To implement QC, one-bit and conditional two-bit gates are required. For any Cooper-pair box, say i, one can shift the flux Φ_{Xi} and/or gate voltage V_{Xi} for a given switching time τ to produce one-bit rotations. A universal set of one-bit gates $U_z^{(i)}(\alpha) = \exp[i\alpha\sigma_z^{(i)}]$, and $U_x^{(i)}(\beta) = \exp[i\beta\sigma_x^{(i)}]$, where $\alpha = -\varepsilon_i(V_{Xi})\tau/\hbar$ and $\beta = \overline{E}_{Ji}\tau/\hbar$, can be defined by choosing $\overline{E}_{Ji} = 0$ and $\varepsilon_i(V_{Xi}) = 0$ in H_1, respectively. Any one-bit rotation can be derived in terms of these two types of one-bit gates. For instance, the Hadamard gate is $R_i = e^{-i\pi/2}U_z^{(i)}(\frac{\pi}{4})U_x^{(i)}(\frac{\pi}{4})U_z^{(i)}(\frac{\pi}{4})$, and the one-bit rotation $V_j = \exp[i\pi\sigma_y^{(j)}/4]$ is given by $V_j = U_z^{(j)}(-\frac{\pi}{4})U_x^{(j)}(\frac{\pi}{4})U_z^{(j)}(\frac{\pi}{4})$. For any two Cooper-pair boxes, say i and j, when $\varepsilon_i(V_{Xi}) = \varepsilon_j(V_{Xj}) = 0$, the Hamiltonian becomes $H_2 = -\overline{E}_{Ji}\sigma_x^{(i)} - \overline{E}_{Jj}\sigma_x^{(j)} - \chi_{ij}\sigma_x^{(i)}\sigma_x^{(j)}$. When the parameters are suitably chosen so that $-\overline{E}_{Ji} = -\overline{E}_{Jj} = \chi_{ij} = \pi\hbar/4\tau$ for a switching time τ, we obtain a conditional two-bit operation: $U' = e^{i\pi/4}U_{2b} = \exp\{i\frac{\pi}{4}[1 - \sigma_x^{(i)} - \sigma_x^{(j)} + \sigma_x^{(i)}\sigma_x^{(j)}]\}$. The controlled-phase-shift gate $U_{\rm CPS}$ is given by $U_{\rm CPS} = R_j^\dagger R_i^\dagger U' R_i R_j$. Combining V_j with $U_{\rm CPS}$, we obtain the controlled-NOT gate: $U_{\rm CNOT} = V_j^\dagger U_{\rm CPS} V_j$. A sequence of such conditional two-bit gates supplemented with one-bit rotations constitute a universal element for QC [8]. Usually, a two-bit operation is much slower than a one-bit operation. Our designs for conditional gates $U_{\rm CPS}$ and $U_{\rm CNOT}$ are efficient since *only one (instead of two or more) two-bit operation* U' *is used.*

The typical switching time $\tau^{(1)}$ during a one-bit operation is of the order $\hbar/E^0_J$. For the experimental value of $E^0_J \sim 100$ mK, there is $\tau^{(1)} \sim 0.1$ ns. The switching time $\tau^{(2)}$ for the two-bit operation is typically of the order $(\hbar/L)(\Phi_0/\pi E^0_J)^2$. Choosing $E^0_J \sim 100$ mK and $\tau^{(2)} \sim 10\tau^{(1)}$ (i.e., ten times slower than the one-bit rotation), we have $L \sim 30$ nH. A small-size inductance with this value can be made with Josephson junctions.

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